REMARKS

Claim 1, for example, calls for forming a trench in each of two semiconductor substrates, at least one of said trenches extending completely across said semiconductor substrates from edge to edge. As to this element, the newly cited reference to Vaiyapuri is applied. It is suggested, citing the material in column 6, that this reference teaches a trench that extends from edge to edge. However, nothing in that material in any way defines how far the trenches, such as the trenches 50 or 70, might extend. However, this is explained better in column 7.

At column 7, lines 35-40, it is explained that the openings to which the cooling channels 50 are formed and the work piece on which the integrated circuit is formed is subjected to a fluid while those openings are sealed. What is unclear is exactly where these openings would be. Could they be openings defined by the trench extending completely across the substrate or are they upward or vertically oriented openings? The next paragraph answers this question. At column 7, lines 49-57, it is explained that the inert fluid 25 is introduced through an opening "preferably through the cavity 70."

Clearly, the cavity 70 is centrally positioned, as shown in Figure 5. If the channels 50 were open because they extended edge to edge or if the cavity 70 extended edge to edge, the fluid would pour out. Instead, it is clear that a vertical filling is accomplished using the more centrally located upward extending via shown in Figure 5 and numbered 70. The fluid stays in, necessarily, because the channels do not extend from edge to edge. Further it is explained in that same material, that an actuator may be laminated over the cavity 70 to subsequently seal the cavity 70. If the channels 50 extended from edge to edge this actuator would not be sufficient to seal them.

Therefore, reconsideration of the rejection of claim 1 and claim 14 is respectfully requested.

Claim 18 calls for combining two substrates using copper to copper bonding and to define a catalyst filled trench between said substrates. The omissions of the other references are allegedly overcome by Burgess that is cited for teaching bonding to substrates using copper to copper bonding. However, nothing in column 6, lines 46-61 suggests any copper to copper bonding. Instead, all that is suggested is that previous direct bonded copper techniques would lead one to assume that the top plate can be manufactured by eliminating beryllia stratum 27 between copper substratum 26 and bottom substratum 28. But none of this teaches any copper to

copper bonding. It seems to discuss bonding beryllia to copper to form a plate, but not to join two semiconductor substrates. Thus, not only does the reference fail to teach copper to copper bonding, it does not even teach using copper to copper bonding to join substrates and, moreover, does not teach using copper to copper bonding to join substrates so as to define a catalyst filled trench between those substrates.

Therefore, reconsideration of the rejection of claim 18 is respectfully requested.

Respectfully submitted,

Date: March 14, 2006

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